



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SR

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/212,291	12/16/98	PRUDVI	C 2207/5915

023838
KENYON & KENYON
1500 K STREET, N.W., SUITE 700
WASHINGTON DC 20005

TM02/0226

EXAMINER

THAI, T

ART UNIT

PAPER NUMBER

2186

DATE MAILED:

9
02/26/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/212,291

Applicant(s)

Prudvi et al.

Examiner

Tuan V. Thai

Group Art Unit

2186

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three (3) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- ☒ Responsive to communication(s) filed on 2/01/01
- ☒ This action is **FINAL**.
- ☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

- ☒ Claim(s) 1-23 is/are pending in the application.
- Of the above claim(s) _____ is/are withdrawn from consideration.
- ☐ Claim(s) _____ is/are allowed.
- ☒ Claim(s) 1-23 is/are rejected.
- ☐ Claim(s) _____ is/are objected to.
- ☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
 - ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been received.
 - ☐ received in Application No. (Series Code/Serial Number) _____.
 - ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

Attachment(s)

- ☒ Information Disclosure Statement(s), PTO-1449, Paper No(s) 8
- ☐ Notice of Reference(s) Cited, PTO-892
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Interview Summary, PTO-413
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Other _____

Office Action Summary

Art Unit: 2186

PART III

RESPONSE TO AMENDMENTS

1. This action is responsive to communication filed on February 01, 2001. This amendment has been entered and carefully considered. Claims 1-23 are presented for examination. Claims 22-23 are newly added.

2. The rejection of claims 1-21 in the Office Action mailed August 18, 2000 (paper # 4) is respectfully maintained, and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 112

3. Claims 1-7 and 11-16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, it has been held that the recitation that an element is "adapted to" (line 1) perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138 (also see other claims; particularly, claim 11, line 4).

Claims which have not mentioned are rejected because they are dependent on the rejected base claims.

Art Unit: 2186

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-23 are rejected under 35 U.S.C. § 102(e) as being anticipated by Chittor et al. (USPN: 6,061,764); hereinafter Chittor.

A processing agent (Chittor Figure 1 Ref No. 10) for transferring data of a predetermined data line in an external transaction (Chittor Figure 1 Ref No. 60 shows a bus which is connected to the processing agent thus allowing it to transfer data in an external transaction), the agent comprising an internal cache having a plurality of cache entries (Chittor Figure 1 ref No. 14 shows the claimed internal cache), each entry for storing multiple data line lengths of data.

The processing agent of claim 1, wherein the cache entries include a cache coherency state field in association with each data line length of data. (Chittor column 5 lines 38-49 teaches

Art Unit: 2186

the claimed cache coherency state field which includes modified, read invalidate etc.);

The agent of claim 1, further comprising a transaction queue having a plurality of queue entries (Chittor Figure 2 ref No. 130 and ref No. 150 teach transaction queues), the queue entries including a primary entry adapted to store address information and status information of a first external transaction and a secondary entry adapted to store status information of a second external transaction (Chittor column 4 lines 5-19 teaches that the queue as claimed holds information pertaining to the address of the transaction as well as status information).

The agent of claim 4, wherein the status information of the first external transaction included a field representing whether the first external transaction is part of a multiple transaction sequence. (Chittor column 5 lines 1-9 teaches that a request is examined and from information which is part of the request (i.e. a field or section of bits within the request) the decoder can determine if the request is part of multiple transactions);

A processing agent (Chittor Figure 1 ref No. 10), comprising a transaction queue having plurality of a queue entries (Chittor figure 2 ref No. 130), the queue entries further comprising;

a primary entry including an address portion and status portion, the status portion provided for a first external transaction of the agent (Chittor figure 2 ref No. 130 is shown

Art Unit: 2186

with multiple entry spaces, also Chittor column 4 lines 5-19 teaches that the queue as claim holds information pertaining to the address of the transaction as well as status information) and

a secondary entry including a status portion provided for second external transaction (Chittor Figure 2 ref No. 130 as written above shows multiple entry lines which each indicate an entry into the queue).

The transaction queue of claim 8, wherein the status portion of the primary entry includes a field representing whether the first transaction is part of a multiple transaction sequence. (Chittor Figure 2 ref No. 130 shows the multiple entry lines within the queue, Chittor column 5 lines 1-9 teaches that a request is examined and from information which is part of the request (i.e. a field or section of bits within the request) the decoder can determine if the request is part of multiple transactions if the request is stored in the queue and the information which tells whether the transaction is part of multiple transaction is part of the request then that data is also stored in an entry within the queue).

The transaction queue of claim 8, further comprising control logic adapted to cycle through the queue entries and post transaction therefrom. (Chittor figure 2 ref No. 110 shows the decode circuit which performs the function of the control logic adapted to cycle through the queue entries.).

Art Unit: 2186

A processing agent (Chittor Figure 1 ref No. 10),
comprising;

an internal cache having entries each adapted to store
multiple data lines, and a transaction related to a single data
line (Chittor figure 1 ref No. 14),

wherein the internal cache and the transaction queue system
each receive data requests on common input (Chittor figure 1 ref
No. 60 is a common input which is connected to the cache as well
as the queue transaction).

The processing agent of claim 11, wherein the internal cache
and the transaction queue system communicate by signal lines
(Chittor figure 1 ref No. 10 shows a signal line from the
processor and cache going to the common bus and Chittor figure 2
shows a line coming from the transaction queue system to the
common bus.).

The processing agent of claim 11, wherein the transaction
queue system comprises a plurality of queue entries, each queue
entry comprising:

a primary entry including an address portion and status
portion, the status portion provided for a first external
transaction of the agent (Chittor figure 2 ref No. 130 shows the
entry within the queue, column 4 lines 5-19 teaches that the
queue as claimed holds information pertaining to the address of

Art Unit: 2186

the transaction as well as status information concerning the transactions), and

a secondary entry including a status portion provided for a second external transaction (Chittor figure 2 ref No. 130 shows the entries within the queue, column 4 lines 5-19 teaches that the queue as claimed holds information pertaining to the address of the transaction as well as status information concerning the transactions).

The transaction queue of claim 14, wherein the status portion of the primary entry includes a field representing whether the first transaction is part of a multiple transaction sequence (Chittor column 5 lines 1-9 teaches that the request is examined and from information which is part of the request (i.e. a field or section of bits within the request) the decoder can determine if the request is part of multiple transactions).

The transaction queue of claim 14, further comprising control logic adapted to cycle through the queue entries and post transaction therefrom (Chittor figure 2 ref No. 110 shows the decode circuit which performs the function of the control logic adapted to cycle through the queue entries.).

As per claims 17-23, they encompass the same scope of invention as to that of the above claims; except that claims 17-21 and 23 are drafted as method format rather than apparatus format. The claims are therefore rejected for the same reasons

Art Unit: 2186

as being set forth above. Noting that Chittor clearly teaches the address field (e.g. see column 5, lines 28 et seq.; and different status fields for indicating and maintaining coherency within Chittor's system (e.g. see column 5, lines 37 et seq.).

6. With respect to the remark; first of all, the size of the cache lines being taught by Chittor to the extent as it is being claimed; for example, as being claimed, the cache entries are sized to store multiple lengths of data; clearly, and as would be understood in memory storage art, the cache lines of Chittor has to include multiple of entries that sized to store multiple data line lengths of data; since Chittor invention directs to variable length read requests from the cache lines wherein *the size of a cache line typically relates to the largest increment of data* (emphasis added) that may be transferred in a single pipelined bus transaction (e.g. see column 2, lines 34 et seq.; column 3, line 8). Secondly, the first and second status portions as being contended by Applicant for claim 8 is also taught by Chittor, for example, Chittor discloses the splitter 140 observes the transaction as it advances out of the inbound transaction queue 130; and from the length field, the splitter 140 determines that the transaction requests data of multiple cache lines. In response, the splitter 140 issues atomic transactions to the bus request generator 122. With one exception, the splitter enables

Art Unit: 2186

an atomic flag with each atomic transaction. The atomic flag is disabled for the final atomic transaction in the series. Thus, the beginning and end of a series of atomic transactions is indicated by the status of the atomic flag (e.g. see column 7, lines 14 et seq.). With regards to other basic concept of cache operation that being omitted in the specification of Chittor wherein cache entries include a tag portion, match detection logic for tag portion to generate cache hit/miss depending on the results of the detection, Examiner wholeheartly believes the invention of Chittor does anticipate those limitations, and Examiner hereby takes Official Notice of those limitations, and gladly provide further information upon requests by Applicant's counsel. For those reasons, Examiner believes that Chittor does anticipate the claimed invention, and the rejection is therefore maintained.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Serial Number: 08/212,291

-10-

Art Unit: 2186

8. Any response to this final action should be mailed to:

Box AF

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications; please
mark "EXPEDITED PROCEDURE")

Or:

(703) 308-6606 (for informal or draft
communications, please label "PROPOSED" or
"DRAFT")

Hand-delivered responses should be brought to Crystal
Park II, 2121 Crystal Drive, Arlington. VA., Sixth
Floor (Receptionist).

9. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for
entry)

Or:

(703) 308-6606 (for informal or draft communications,
please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal
Park II, 2121 Crystal Drive, Arlington. VA., Sixth
Floor (Receptionist).

10. Any inquiry concerning this communication or earlier
communications from the examiner should be directed to Tuan V.
Thai whose telephone number is 703-305-3842.

Serial Number: 08/212,291

-11-

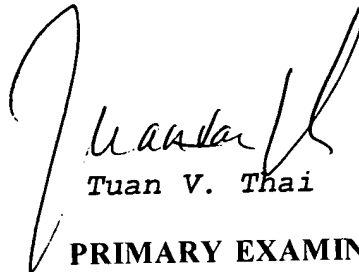
Art Unit: 2186

The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM. The examiner can also be reached on alternate Fridays or e-mailed at *tuan.thai@uspto.gov*;

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Matthew M. Kim can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TVT/February 22, 2000



Tuan V. Thai

PRIMARY EXAMINER

Group 2100